(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 536 758 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **92117221.9**

(51) Int. Cl.5: **G09G 3/36**

(22) Date of filing: **08.10.92**

(30) Priority: **08.10.91 JP 260188/91**

(43) Date of publication of application:
14.04.93 Bulletin 93/15

(84) Designated Contracting States:
DE FR GB

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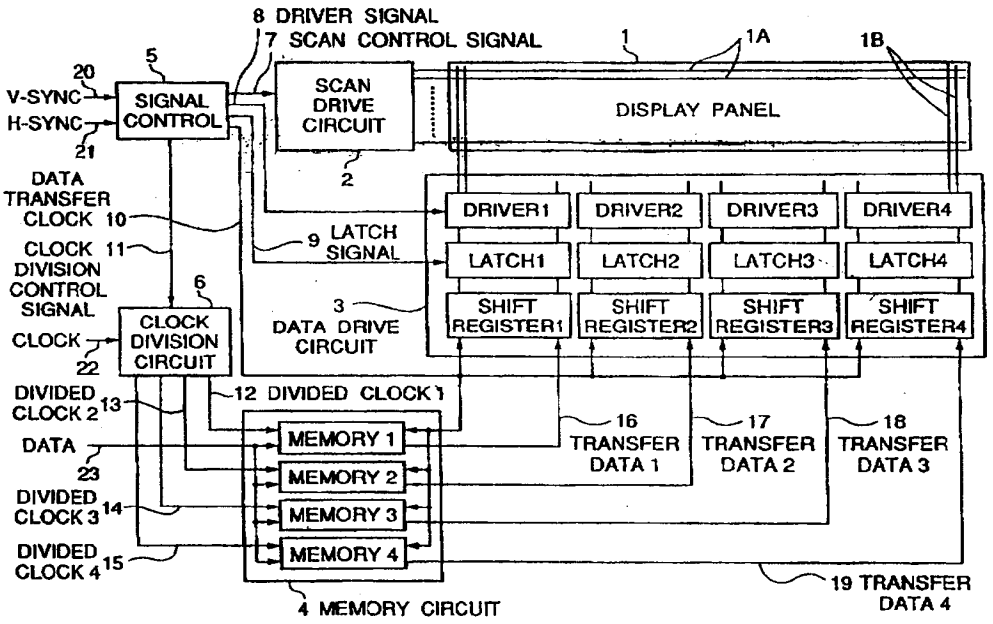
(54) Display apparatus having shift register of reduced operating frequency.

(57) In a dynamic drive type matrix display apparatus having a scan drive circuit for sequentially driving a number of scan electrodes of a display panel and a data drive circuit for simultaneously driving a number of data electrodes of the display panel, the data drive circuit is divided into a plurality of data drive sub-circuits, and data of one scan to be transferred to a shifter register of each of the data drive sub-circuits is stored in a memory circuit once, and thereafter, simultaneously transferred in parallel to the shift registers of all the data drive sub-circuits.

FIGURE 1



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Background of the Invention

Field of the invention

The present invention relates to a display apparatus, and more specifically to a data transfer system for transferring data to a data drive circuit of a dynamic drive type display apparatus.

Description of related art

A typical conventional display apparatus includes a signal control circuit receiving a vertical synchronizing signal and a horizontal synchronizing signal and generating a scan control signal, a driver signal and a latch signal. In response to the scan control signal, a scan drive circuit sequentially drives a number of scan electrodes of a display panel. On the other hand, a data drive circuit receives a data signal and a clock signal and is controlled by the driver signal and the latch signal so as to drive a number of data electrodes of the display panel. The data drive circuit is composed of for example a driver, a latch and a shift register. The clock signal is a dot clock in synchronism with the data signal.

With the above arrangement, the display panel is driven in a line sequential scanning manner from a first line to a final line in accordance with the horizontal synchronizing signal, and this scanning is repeated with reference to the vertical synchronizing signal. For this purpose, during one period of the horizontal synchronizing signal, a number of items of data corresponding to display cells of one scan line line are serially supplied to the shift register of the data drive circuit in synchronism with the clock signal, and after the data has been written to the shift register, a content of the shift register is transferred from a parallel output of the shift register to the latch. The display cells on one scan line selected by the scan drive circuit is energized or deenergized by the driver of the data drive circuit on the basis of the data held in the latch during one period of the horizontal synchronizing signal, namely, in one scanning period.

The above mentioned conventional display apparatus is such that the data signals are serially transferred to the shift register. Therefore, since a required frequency of the clock signal and the data signal increases in proportion with increase of a display capacity, the shift register having a high operating frequency has been required.

Summary of the Invention

Accordingly, it is an object of the present invention to provide a display apparatus which has overcome the above mentioned defect of the conventional one.

Another object of the present invention is to provide a data drive circuit for use in a dynamic drive type display apparatus, which has a large display capacity but can use a shift register having a low operating frequency.

The above and other objects of the present invention are achieved in accordance with the present invention by a display apparatus so configured that a display voltage is sequentially applied to scan electrodes from a scan drive circuit, and data items corresponding to the number of cells of one scan line are transferred to a shift register, and after completion of the data transfer, all data of the shifter register is shifted to a latch, so that a voltage determining energization/deenergization of a display cell is applied from a data drive circuit in accordance with data latched in the latch, the display apparatus being characterized in that the data drive circuit is divided into a plurality of data drive sub-circuits, and data of one scan to be transferred to a shifter register of each of the data drive sub-circuits is stored in a memory circuit once, and thereafter, simultaneously transferred in parallel to the shift registers of all the data drive sub-circuits.

In a preferred embodiment, the matrix display apparatus includes:

a display panel having a number of scan electrodes, a number of data electrodes and a number of display cells formed at intersections between the scan electrodes and the data electrodes;

scan drive means receiving a vertical synchronizing signal and a horizontal synchronizing signal for sequentially driving the scan electrodes;

data drive means including at least shift register means and for driving the data electrodes on the basis of a content of the shift register means, the shift register means includes a plurality of shift registers each of which has a serial data input;

memory means including a corresponding number of memories each of which has a data input receiving a data signal in common and a data output connected to the serial data input of a corresponding one of the shift registers; and

control means receiving a clock signal for controlling the memories and the shift registers so that the data signal is sequentially distributed to the memoirs and the respective data signals stored in the memories are simultaneously supplied to all the shift registers.

More specifically, the control means includes a signal control circuit receiving the vertical synchronizing signal and the horizontal synchronizing signal for generating a data transfer signal, which is supplied in parallel to the shift registers as a write control signal and is also supplied in parallel to the memories as a read control signal, and a clock division circuit receiving the clock signal for gen-

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erating a corresponding number of frequency-divided clocks which are different in phase from one another and each of which is supplied to a corresponding one of the memories as a write control signal.

The above and other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a block diagram showing one embodiment of the matrix display apparatus in accordance with the present invention;

Figure 2 is a timing chart illustrating an operation of the embodiment shown in Figure 1, in the case of having the display capacity of 640 × 400 dots; and

Figure 3 is a block diagram showing another embodiment of the matrix display apparatus in accordance with the present invention.

Description of the Preferred embodiments

Referring to Figure 1, there is shown a block diagram showing one embodiment of the dynamic drive type matrix display apparatus in accordance with the present invention.

The shown dynamic drive type matrix display apparatus includes a signal control circuit 5 which receives a vertical synchronizing signal 20 and a horizontal synchronizing signal 21 and generates a scan control signal 7, a driver signal 8, a latch signal 9, a data transfer clock 10 and a clock division control signal 11. In response to the scan control signal 7, a scan drive circuit 2 sequentially drives a number of scan electrodes 1A of a display panel 1. On the other hand, a data drive circuit 3 receives the driver signal 8, the latch signal 9 and the data transfer clock 10 and also receives data from a memory circuit 4 for driving a number of data electrodes 1B of the display panel 1. Display cells are constituted in intersections between the scan electrodes 1A and the data electrodes 1B.

The shown embodiment also includes a clock division circuit 6 which receives a clock signal 22 and a clock division control signal 11 and which time-divides the clock signal 22 into four divided clock signals 12 to 15 labelled with "DIVIDED CLOCK 1" to "DIVIDED CLOCK 4" on the basis of the clock division control signal. These divided clock signals 12 to 15 are different in phase from one another.

A memory circuit 4 includes four memories labelled with "MEMORY 1" to "MEMORY 4". A data signal 23 is connected in parallel to the four memories "MEMORY 1" to "MEMORY 4", which also receive the four divided clock signals 12 to 15, respectively, as a write control signal. Therefore, the data signal 23 is distributed and written into memories "MEMORY 1" to "MEMORY 4" in response to the divided clock signals 12 to 15.

The four memories "MEMORY 1" to "MEMORY 4" also receive the data transfer clock 10 as a read control signal, so that four transfer data 16 to 19 labelled with "TRANSFER DATA 1" to "TRANSFER DATA 4" are simultaneously read from the four memories "MEMORY 1" to "MEMORY 4" in response to the data transfer clock 10.

The data drive circuit 3 includes four data drive sub-circuits, each of which includes one driver, one latch and one shift register. In the drawing, the driver, the latch and the shift register of a first data drive sub-circuit are labelled with "DRIVER 1", "LATCH 1" and "SHIFT' REGISTER 1", respectively. In a second data drive sub-circuit, the driver, the latch and the shift register are labelled with "DRIVER 2", "LATCH 2" and "SHIFT REGISTER 2", respectively. In a third data drive sub-circuit, the driver, the latch and the shift register are labelled with "DRIVER 3", "LATCH 3" and "SHIFT REGISTER 3", respectively. In a fourth data drive sub-circuit, the driver, the latch and the shift register are labelled with "DRIVER 4", "LATCH 4" and "SHIFT REGISTER 4", respectively. The driver signal 8 is supplied to the drivers of all the first to fourth data drive sub-circuits, and the respective drivers of the first to fourth data drive sub-circuits are simultaneously drive all the data electrodes 1B of the display panel 1 in parallel. The latch signal 9 is also supplied to the latches of all the first to fourth data drive sub-circuits, and the data transfer clock 10 is supplied as a write control signal to the shift registers of all the first to fourth data drive sub-circuits, which are connected to receive at their serial input a corresponding one of the four transfer data "TRANSFER DATA 1" to "TRANSFER DATA 4".

With the above mentioned arrangement, the serially supplied data signal 23 is distributed by the divided clock signals 12 to 15 "DIVIDED CLOCK 1" to "DIVIDED CLOCK 4" to the four memories "MEMORY 1" to "MEMORY 4" corresponding to the four shift registers "SHIFT REGISTER 1" to "SHIFT REGISTER 4". Thus, the data for the shift register 1 is stored in the memory 1, and the data for the shift register 2 is stored in the memory 2. In addition, the data for the shift register 3 is stored in the memory 3, and the data for the shift register 4 is stored in the memory 4. The data stored in the memories 1 to 4 is simultaneously read out in response to the data transfer clock 10, so as to constitute the transfer data 16 to 19. Therefore, the

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frequency of the transfer to the shift registers "SHIFT REGISTER 1" to "SHIFT REGISTER 4" is determined by the data transfer clock 10. Since the data signal 23 is converted or distributed into four parallel bits of the transfer data 1 to 4, the data transfer clock 10 can be made to one fourth of the frequency of the clock signal 22.

Figure 2 shows a timing chart illustrating a relation between the input signal, the data transfer clock, the transfer data 1 to 4, and the display in the embodiment having the display capacity of 640 × 400 dots. During each one period of the horizontal synchronizing signal, there exist the data transfer clocks of 160 pulses which is one fourth of 640. Therefore, the data transfer clock has a frequency obtained by frequency-dividing the clock signal. The transfer data 1 to 4 is the signals read out from the memory circuit 4 after the data signals had been stored once in the memory circuit 4, and therefore, is delayed from the data signal by one period of the horizontal synchronizing signal. Accordingly, the display is performed with a further delay corresponding to one period of the horizontal synchronizing signal.

Referring to Figure 3, there is shown a block diagram showing another embodiment of the matrix display apparatus in accordance with the present invention. In Figure 3, elements similar to those shown in Figure 1 are given the same Reference Numerals, and explanation thereof will be omitted.

As seen from comparison between Figures 1 and 3, the second embodiment is characterized in that the four drivers "DRIVER 1" to "DRIVER 4" and the four latches "LATCH 1" to "LATCH 4" are replaced with one driver "DRIVER" and one latch "LATCH", respectively.

In the present invention, it is important that the shift register of the data drive circuit is divided into a plurality of shift registers which can receives different data signals in parallel. Therefore, the second embodiment operates similarly to the first embodiment.

As mentioned above, the present invention can lower the transfer rate of the data to the shift register of the data drive circuit, since the data drive circuit has a plurality of shift registers, and since there is provided a converting circuit used for transferring the data into respective shift registers in parallel. In addition, if the frequency-dividing number for the data transfer rate is made lower than the dividing number of the data drive circuit, namely, the number of the shift registers, the processing time for transferring data to the shift registers can be lowered.

The invention has thus been shown and described with reference to the specific embodiments. However, it should be noted that the present invention is in no way limited to the details of the illustrated structures but changes and modifications may be made within the scope of the appended claims.

Claims

1. A display apparatus so configured that a display voltage is sequentially applied to scan electrodes from a scan drive circuit, and data items corresponding to the number of cells of one scan line are transferred to a shift register, and after completion of the data transfer, all data of the shifter register is shifted to a latch, so that a voltage determining energization/deenergization of a display cell is applied from a data drive circuit in accordance with data latched in the latch, characterized in that said data drive circuit is divided into a plurality of data drive sub-circuits, and data of one scan to be transferred to a shifter register of each of said data drive sub-circuits is stored in a memory circuit once, and thereafter, simultaneously transferred in parallel to the shift registers of all said data drive sub-circuits.

2. A matrix display apparatus includes:

   a display panel having a number of scan electrodes, a number of data electrodes and a number of display cells formed at intersections between said scan electrodes and said data electrodes;

   scan drive means receiving a vertical synchronizing signal and a horizontal synchronizing signal for sequentially driving said scan electrodes;

   data drive means including at least shift register means and for driving said data electrodes on the basis of a content of said shift register means, said shift register means includes a plurality of shift registers each of which has a serial data input;

   memory means including a corresponding number of memories each of which has a data input receiving a data signal in common and a data output connected to said serial data input of a corresponding one of said shift registers; and

   control means receiving a clock signal for controlling said memories and said shift registers so that said data signal is sequentially distributed to said memoirs and the respective data signals stored in said memories are simultaneously supplied to all said shift registers.

3. A matrix display apparatus claimed in Claim 2 wherein said control means includes a signal control circuit receiving said vertical synchro-

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nizing signal and said horizontal synchronizing signal for generating a data transfer signal, which is supplied in parallel to said shift registers as a write control signal and is also supplied in parallel to said memories as a read control signal, and a clock division circuit receiving said clock signal for generating a corresponding number of frequency-divided clocks which are different in phase from one another and each of which is supplied to a corresponding one of said memories as a write control signal.

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FIGURE 1

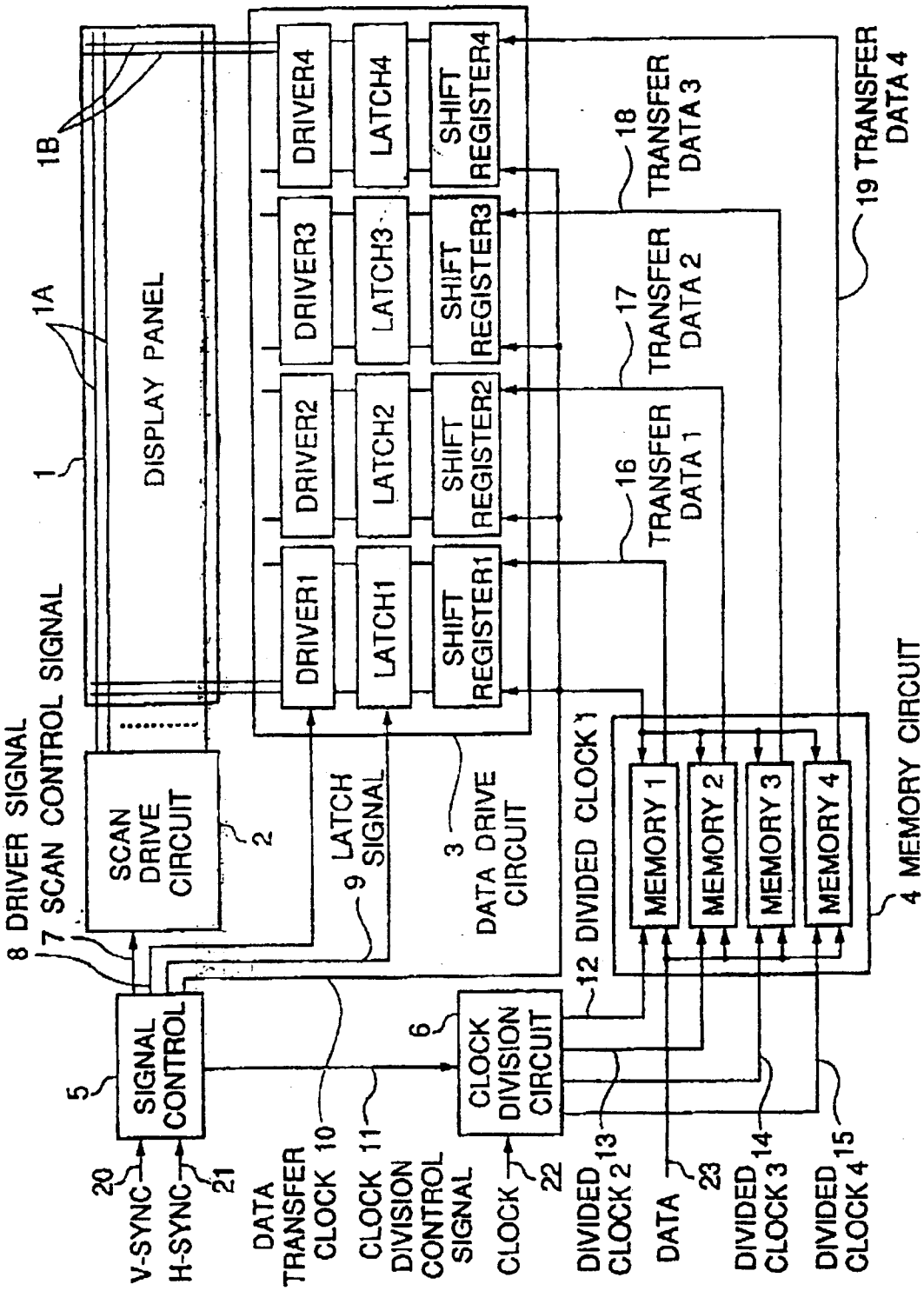

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FIGURE 2

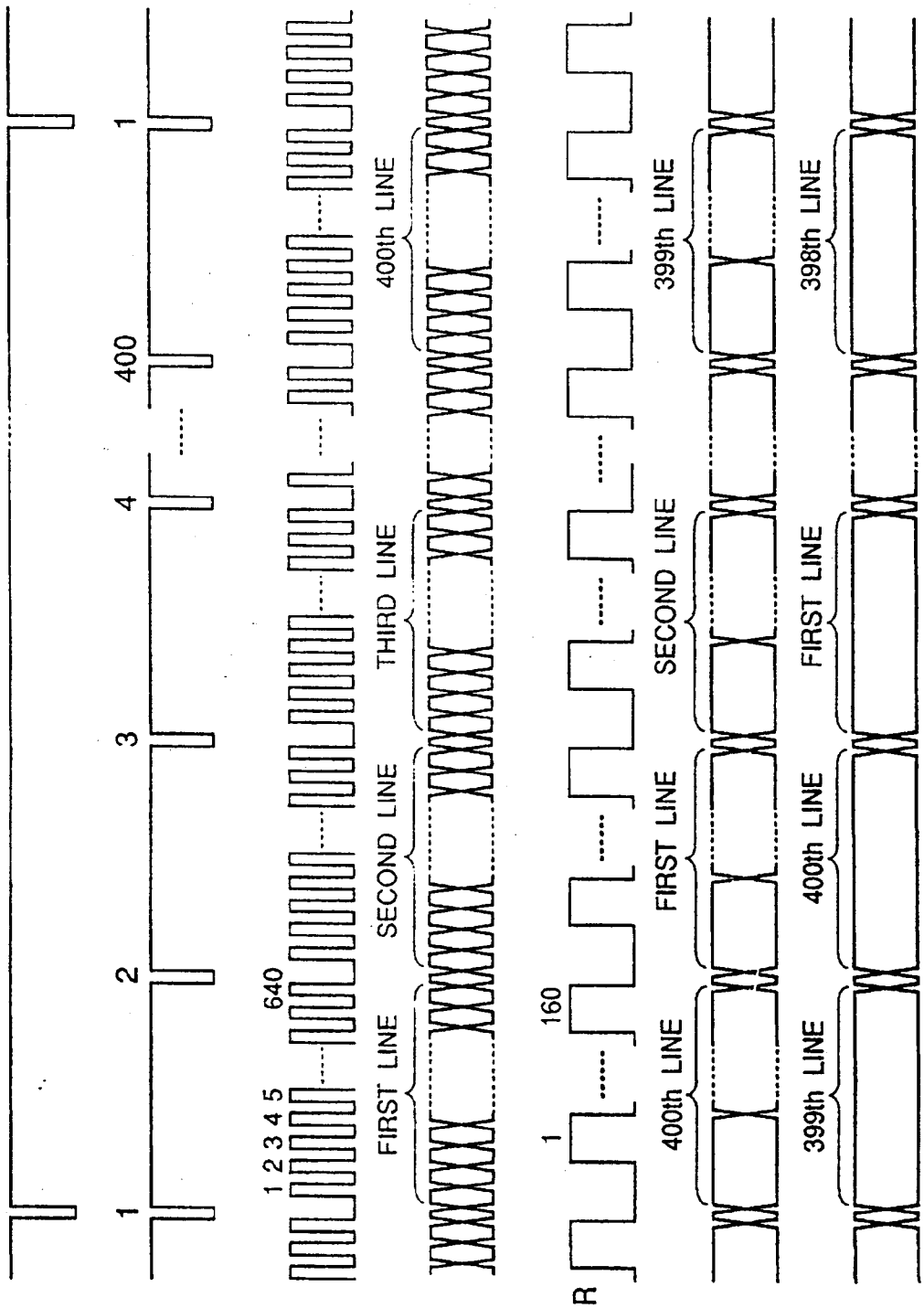

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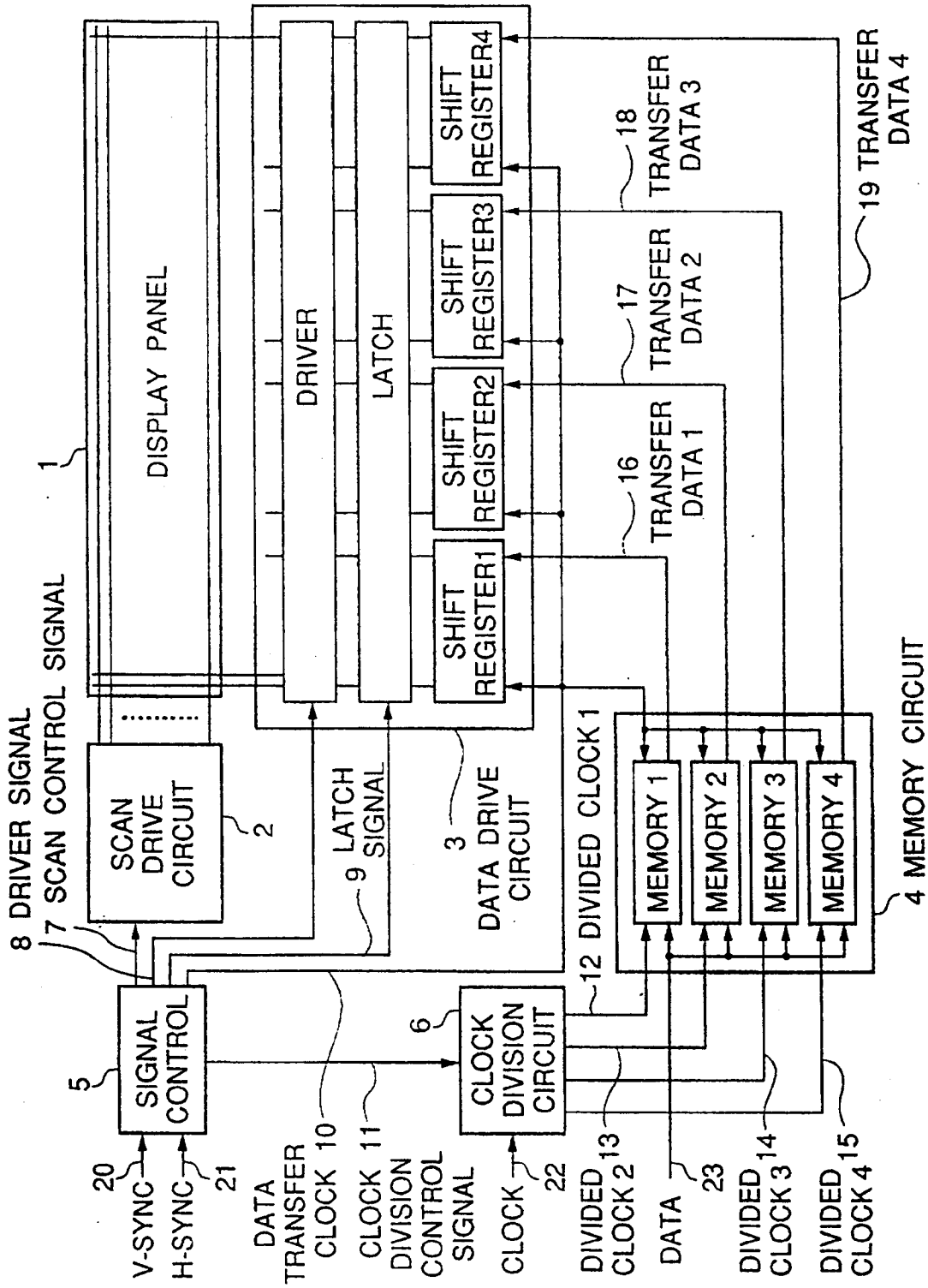
FIGURE 3



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EUROPEAN SEARCH REPORT

Application Number

EP 92 11 7221

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 149 151 (Y. NAGAE ET AL.) * column 5, line 55 - column 7, line 5; figures 7-9 *	1,2	G09G3/36
A	GB-A-2 135 099 (CITIZEN) * abstract; figure 9 * * page 1, line 58 - line 90 *	1-3	
A	GB-A-2 170 033 (APPLE) * abstract; figures 1,6 * * page 2, line 20 - line 45 *	1-3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	05 JANUARY 1993	SAAM C.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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